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Remarks

Applicant and his representatives wish to thank Examiner Sullivan for the thorough examination of the present application and the detailed explanations in the Office Action dated December 7, 2006. Applicant's undersigned representative also wishes to thank Examiner Sullivan and Supervisory Primary Examiner Huff for the very helpful and courteous discussion held on March 22, 2007. The claims have been amended as discussed, and certain excerpts from Wolf et al., *Silicon Processing for the VLSI Era*, vol. 4 (Lattice Press, Sunset Beach, California [2002]) disclosing well-known void formation phenomena are submitted herewith (see the accompanying Information Disclosure Statement). The following remarks shall further summarize and expand upon topics discussed.

The present invention relates to a method for forming a metal line. The method (as set forth in amended Claim 1 above) generally comprises:

- a) stacking a lower insulating layer, a lower metal line and an upper insulating layer;
- b) patterning a first photosensitive film on the upper insulating layer;
- c) using the patterned first photosensitive film as a mask, etching the upper insulating layer until at least a portion of the lower metal line is exposed;
- d) filling an etched portion of the upper insulating layer with a nitride film;
- e) patterning a second photosensitive film over the lower metal line and the nitride film;
- f) using the second photosensitive film as a mask, etching the lower metal line until the lower insulating layer is exposed to form a lower metal line pattern;
- g) depositing an IMD (Inter Metal Dielectric) layer on the lower metal line pattern and the nitride film, thereby forming an air gap in the IMD layer between lines in the lower metal line pattern;

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- h) planarizing the IMD layer to expose the nitride film;
- i) removing the nitride film, thereby forming a contact hole in the IMD layer exposing an upper surface of the lower metal line;
- j) filling the contact hole with a conductive material; and
- k) depositing an upper metal line over the conductive material.

The references cited against the originally-filed claims (Furukawa et al, U.S. Pat. No. 6,221,704 [hereinafter "Furukawa"], Wang, U.S. Pat. No. 6,159,840 [hereinafter "Wang"], Grill et al., U.S. Pat. No. 6,737,725 [hereinafter "Grill"], and Gardner et al., U.S. Pat. No. 5,869,379 [hereinafter "Gardner"]) neither disclose nor suggest filling the etched portion of an insulating layer exposing a portion of a lower metal line with a nitride film, depositing an IMD layer on the lower metal line pattern and the nitride film, thereby forming an air gap in the IMD layer between lines in the lower metal line pattern, and removing the nitride film, thereby forming a contact hole in the IMD layer (see amended Claim 1). Consequently, the present claims are patentable over the cited references.

The Rejection of Claims 1-6 under 35 U.S.C. § 112, First Paragraph

The rejection of Claims 1-6 under 35 U.S.C. § 112, second paragraph, is, in part, obviated by appropriate amendment, and is, in part, respectfully traversed.

The specification describes how to form an air gap (or "void," as it is also known in the art) in a dielectric material. The specification clearly discloses (and FIG. 2E of the present application clearly shows) depositing an IMD (Inter Metal Dielectric) layer 212 over an entire structure, thereby forming an air gap 214 within the IMD layer 212 (also see paragraph [0015] on page 4 of the present specification). As taught by Wolf (see the reference submitted with the attached Information Disclosure Statement), it is well-known in the art that voids can be formed in a dielectric deposited onto metal lines (pp. 322-323) or into trenches in a semiconductor

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substrate (pp. 458-462). Thus, the formation of air gaps (or voids) in a dielectric material deposited onto metal lines is well-known in the art.

Claim 1 has also been amended to recite forming an air gap in the IMD layer as part of the step of depositing the IMD (Inter Metal Dielectric) layer on the lower metal line pattern and the nitride film. As a result, this ground of rejection is no longer sustainable, and notice of its withdrawal is respectfully requested.

The Rejection of Claims 1-6 under 35 U.S.C. § 103(a)

The rejection of Claims 1-6 under 35 U.S.C. § 103(a) as being unpatentable over Furukawa and Wang, in view of Grill and Gardner is respectfully traversed.

Furukawa discloses a process for fabricating a short channel field effect transistor with a highly conductive gate (Title). Furukawa teaches removing a portion of a second insulating layer 5 located beneath an opening in a photoresist layer 6 down to conductive forming layer 4 (col. 6, ll. 38-40, and FIG. 4). However, Furukawa discloses only doped polysilicon or intrinsic polysilicon with doping ions implanted into it (essentially the same thing as doped polysilicon) as the conductive forming layer 4 (col. 3, ll. 42-59, and FIGS. 1-3). Thus, Furukawa does not disclose stacking *a lower insulating layer, a lower metal line* and an upper insulating layer, as recited in Claim 1.

One may try to read conductive material layer 7 of Furukawa on the lower metal line of the present Claim 1. However, the conductive material layer 7 of Furukawa is formed by filling the trench created in insulating layer 5 with the conductive material, much like the nitride film recited in the present Claim 1. Thus, if one reads the conductive material layer 7 of Furukawa on the lower metal line recited in the present Claim 1, then Furukawa fails to disclose planarizing an IMD layer to expose the nitride film, removing the nitride film to thereby form a contact hole in the IMD layer exposing an upper surface of the lower metal line, or filling the contact hole with a conductive material, as recited in the present Claim 1.

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However, Furukawa retains the conductive material layer 7 in the final gate structure (see FIG. 4 and col. 7, ll. 27-30). Thus, Furukawa truly fails to disclose planarizing an IMD layer to expose the nitride film, removing the nitride film to thereby form a contact hole in the IMD layer exposing an upper surface of the lower metal line, or filling the contact hole with a conductive material, as recited in the present Claim 1. In addition, Furukawa is silent with regard to voids and/or air gaps in a dielectric layer (see Claim 1 above). Thus, Furukawa is saliently deficient with regard to amended Claim 1.

Wang discloses forming a metal layer 202 on the substrate 200 as the bottom layered conductive line of the metal interconnect (col. 2, ll. 49-51 and FIGS. 1 and 2A). A dielectric layer 204 is further formed covering the metal layer 202 and the substrate 200, and thereafter, a stop layer 206 is formed on the dielectric layer 204 (for example, a silicon nitride layer; see col. 2, ll. 51-57 of Wang). A dielectric layer 208 (for example, an oxide layer) is further formed on the stop layer 206 (col. 2, ll. 57-59 of Wang).

Wang then teaches defining the dielectric layer 208, the stop layer 206 and the dielectric layer 204 using the photoresist layer 210, followed by removing the portions of the dielectric layer 208, the stop layer 206 and the dielectric layer 204 not covered by the photoresist layer 210 to form a via opening 212a and an opening 212b where the air-gap is to be formed (col. 2, ll. 60-67 and FIGS. 1 and 2B). Wang then forms a dielectric material 214 (such as a PECVD oxide layer) on the dielectric layer 208 (col. 3, ll. 7-9 and FIG. 2C). The recipe for forming the dielectric material 214 is adjusted during the deposition process to result in a dielectric material 214 with a slightly inferior step coverage property. The dielectric material 214 thus directly covers the dielectric layer 208, scaling the opening 212b (as in FIG. 2B) to form an air gap 213, but not completely filling the opening 212b (col. 3, ll. 10-15 of Wang). Furthermore, the dielectric material 214 also covers the via opening 212a, resulting in a part of the dielectric material 214 partially filling the via opening 212a. The height of the dielectric material 214 in the via opening 212a and the opening 212b is controlled to be above the stop layer 206, which is favorable in forming the air-gap 213 and manufacturing the via plug (col. 3, ll. 15-22 of Wang).

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Wang then forms a photoresist layer 216 on the dielectric material 214, and forms a trench 218 in the dielectric material 214 and the dielectric layer 208 (see FIGS. 2D-2E and col. 3, ll. 23-27 of Wang). The trench 218 is formed by anisotropic etching of the dielectrics 214 and 208 using the stop layer 206 as an etch-stop. The dielectric material 214 and the dielectric layer 208 are completely removed in the via opening 212a to expose the metal layer 202. On the other hand, the dielectric material 214 above the air-gap 213, protected by the photoresist layer 216, remains (col. 3, ll. 27-37 and FIG. 2E of Wang).

Thus, like Furukawa, Wang fails to disclose planarizing an IMD layer to expose the nitride film, removing the nitride film to thereby form a contact hole in the IMD layer exposing an upper surface of the lower metal line, or filling the contact hole with a conductive material, as recited in the present Claim 1. In addition, Wang fails to disclose filling an etched portion of the upper insulating layer with a nitride film. Grill and Gardner fail to cure the salient deficiencies of Furukawa and Wang.

Grill discloses a method for forming a multilayer interconnect structure that includes interconnected conductive wiring and vias spaced apart by a combination of solid or gaseous dielectrics (Abstract, ll. 1-4). The method includes the steps of: (a) forming a first planar via plus line level pair embedded in a dielectric matrix formed from one or more solid dielectrics, wherein at least one of said solid dielectrics is at least partially sacrificial; (b) etching back sacrificial portions of the sacrificial dielectrics to leave cavities extending into and through the via level, while leaving at least some of the original via level dielectric as a permanent dielectric under the lines; (c) partially filling or overfilling the cavities with a place-holder material; (d) planarizing the structure by removing overfill of the place-holder material; (e) repeating steps (a)-(d) as necessary; (f) forming a dielectric bridge layer over the planar structure; and (g) forming air gaps by at least partially extracting the place-holder material (Abstract, ll. 4-end).

Grill teaches that the structure of FIG. 1G (containing wiring structures 185) is overfilled with a sacrificial place-holder (SPH) material 220 to form the structure of FIG. 1H (col. 6, ll. 20-45). It is preferred that the SPH be a material that "gap fills" in a way *that does not leave cavities* that will be opened when the SPH is planarized (col. 6, ll. 50-53). After forming the

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desired number of wiring and via levels (i.e., patterned conductors embedded in a dielectric matrix comprising permanent dielectric materials and SPH materials; see col. 7, ll. 1-5 and FIG. 1L), dielectric bridge layer 250 is formed and patterned with small openings (holes or perforations) 260 to produce the structure of FIG. 1M (see col. 7, ll. 5-7 of Grill). SPH material 220' and 220 in FIG. 1M is then extracted to form the structure of FIG. 1N, with air gaps 270 (col. 7, ll. 35-36).

Like Furukawa and Wang, Grill fails to disclose filling an etched portion of an upper insulating layer with a nitride film, planarizing an IMD layer to expose the nitride film, and removing the nitride film to thereby form a contact hole in the IMD layer and expose an upper surface of the lower metal line. Like Furukawa, Grill fails to disclose depositing an IMD layer on the lower metal line pattern and the nitride film, thereby forming an air gap in the IMD layer between lines in the lower metal line pattern. Thus, Grill fails to cure the salient deficiencies of Furukawa and Wang with regard to the method recited in amended Claim 1.

Like Furukawa, Gardner discloses a process for forming a transistor (Abstract, l. 1). an Gardner teaches that an isotropic etch may be performed on exposed lateral surfaces of polysilicon gate conductors 18 such that the gate conductors are selectively narrowed to a pre-determined lateral thickness (see col. 5, ll. 46-49 and FIG. 6). While masking structures 20 are preferably composed of nitride, they may comprise oxide, silicon oxynitride, or a metal. Thus, depending on whether masking structures 20 are nitride or a metal, Gardner discloses either filling an etched portion of the upper insulating layer with a nitride film or stacking a lower insulating layer, a lower metal line and an upper insulating layer. It appears that Gardner cannot disclose both.

Furthermore, Gardner appears to be silent with regard to removing masking structures 20, forming structures that replace masking structures 20, or forming structures that are over such replacement structures. Therefore, like Furukawa, Wang and Grill, Gardner fails to disclose removing a nitride film to thereby form a contact hole in an IMD layer and expose an upper surface of the lower metal line (or any step subsequent thereto), as recited in the present Claim 1.

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As a result, no possible combination of the cited references discloses or suggests removing a nitride film to thereby form a contact hole in an IMD layer and expose an upper surface of the lower metal line (or steps associated therewith), as recited in amended Claim 1 above. Consequently, this ground of rejection is unsustainable, and should be withdrawn.

The Rejection of Claims 1-6 under 35 U.S.C. § 112, Second Paragraph

The rejection of Claims 1-6 under 35 U.S.C. § 112, second paragraph, has been obviated by appropriate amendment.

Conclusions

In view of the above amendments and remarks, all bases for objection and rejection are overcome, and the application is in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,



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